REMARKS/ARGUMENTS

1. Amendments to the Specification

Original specification paragraphs [0027] – [0029] are amended to correct typographical/grammatical errors. Since the searched programming codes could be transmitted to the microprocessor, the whole access process of accessing these requested programming codes can be speeded up accordingly.

Original specification paragraph [0043] is amended to support the features recited in claim 31.

A new paragraph [0043.1] is added to support features recited in claims 3, 7, 10, 14, 18, 22, 27, and 37.

No new matter is introduced. Consideration of these specification amendments is respectfully requested.

2. Amendments to the Claims

Claim 1 is amended to include limitations recited in claim 4, and claim 4 is amended to delete the limitations incorporated into claim 1 accordingly. Dependent claims are amended in response to amendments made to claims 1 and 4.

Claim 8 is amended to include limitations recited in claim 11, and claim 11 is amended to delete the limitations incorporated into claim 8 accordingly. Dependent claims are amended in response to amendments made to claims 8 and 11.

Claim 16 is amended to include limitations recited in claim 19, and claim 19 is amended to

delete the limitations incorporated into claim 16 accordingly. Dependent claims are amended in response to amendments made to claims 16 and 19.

Claim 32 is amended and the newly entered claim 39 includes the limitation originally recited in claim 32.

Regarding claims 7, 14, 22, and 37, because the specification discloses that the buffering/controlling device has the ability of buffering programming codes requested by the microprocessor and controlling the operating clock of the microprocessor, the buffering/controlling device therefore must comprise a storage component for data buffering.

Regarding claims 3, 10, 18, and 27, they are amended to clearly define what applicants intend to mean.

No new matter is introduced. Consideration of these claim amendments is respectfully requested.

3. Rejections: 35 U.S.C. 112, 1st PARAGRAPH

Claims 1-38 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

1) Independent claims 1, 8, and 16 have limitations directed toward the data stored in either a serial flash memory or a random access memory being either 'well prepared' or 'not well prepared'. This language is not explained in the specification or drawings. This language is not typically used in describing data in memory devices and with an absence within the

specification of the language being further clarified, the meaning of the language cannot be determined.

Response:

Claims 1, 8, 16 have been amended. Applicants believe that the amended claims 1, 8, and 16 have complied with the enablement requirements.

2) Independent claim 24 has limitations which state 'reducing an executing speed of the microprocessor emulator for a certain period' and 'executing the microprocessor emulator at a normal speed after the certain period', however, this language is not explained in the specification or drawings. The 'certain period' is not defined in the specification and this time period cannot be determined from either the specification or the drawings.

Response:

As stated in specification paragraph [0040], "Concerning the previous embodiments shown in Fig.3 and Fig.4, the microprocessor emulator 54 corresponds to the microprocessor 30. In order to make the microprocessor emulator 54 authentically emulate the operation of the microprocessor system 50 of the present invention, the buffering/controlling device 58 provides an operating clock to the microprocessor emulator 54 so as to control the microprocessor emulator 54," it can be readily understood that the microprocessor emulator 54 emulates operations of the microprocessor 30. Additionally, as shown in Fig.5 and illustrated in specification paragraph [0030], the covering mask signal has a 'certain period' to reduce the executing speed by slowing/stopping the operating clock outputted to the microprocessor, and the normal executing speed is resumed after the 'certain period'. Therefore, applicants believe that original claim 24 has complied with the enablement requirements.

3) Further elements used in the specification require some type of definition or explanation because these elements are not clearly defined in the memory arts. Examples are:

a) buffering/controlling device – the specification does not define what type of devices are used for this buffering/controlling device, they are not typically the same element in a memory circuit;

Response:

Because the specification clearly states that the buffering/controlling device is able to buffer programming codes and control the operating clock, a person skilled in this art can readily understand that any components or combinations thereof capable of providing these functions can be adopted to implement the buffering/controlling device. Therefore, applicants believe that the buffering/controlling device has been clearly defined by its operation and functionality.

b) microprocessor-operating-speed control device – the specification does not define or explain what comprises this device;

Response:

The microprocessor-operating-speed control device can be implemented by any components capable of controlling the operating speed of the microprocessor as indicated by the naming. Therefore, applicants believe that the microprocessor-operating-speed control device is clearly defined by the naming of this term.

c) outputs an operating clock – clock signals are output by some elements but the operating clock itself is not 'output';

Response:

As known to those skilled in this art, the microprocessor is operated according to an incoming clock signal. Commonly, this clock signal serves as the operating clock of the microprocessor directly. Therefore, it is clear and known to those skilled in this art to define that the operating clock is outputted from the buffering/controlling device to the microprocessor.

d) the specification does not define a 'data clog';

Response:

The 'data clog' is a term commonly used in the data transmission, and can be found in many references. Applicants believe that there is no need to define this term since it is well known to those skilled in pertinent art.

e) how does the operating clock disappear, what does this mean in relationship to actual circuitry;

Response:

As shown in Fig.5 of this application, the operating clock is stopped (gated) in a period when the covering mask signal has a high voltage level. Because no clock pulses are inputted to the microprocessor, the microprocessor is halted. In other words, the operating clock disappears in this period controlled by the covering mask signal. Any clock gating techniques can be implemented to make the operating clock disappear. After reading the operations described in the specification, a person skilled in this art can readily understand how to make the operating clock disappear. Applicants believe that there is no need to define this operation in detail since how to make a clock signal disappear is well known to those skilled in pertinent art.

f) how is that operating clock recovered, what does this mean in relationship to actual circuitry;

Response:

As shown in Fig.5 of this application, the operating clock has clock pulses again after the covering mask signal is reset to another predetermined voltage level. Since the clock pulses are inputted to the microprocessor again, the microprocessor continues processing the interrupted tasks. Similarly, after reading the operations described in the specification, a person skilled in this art can readily understand how to recover the operating clock. Applicants believe that there is no need to define this operation in detail since how to recover a clock signal is well known to those skilled in pertinent art.

g) what is meant by 'fasten the whole access process', the 'whole process' is not defined in the specification and if the term should be 'faster' and not 'fasten' it is not explained how the 'whole process' is faster.

Response:

The typographical errors in the specification have been corrected. Additionally, since the searched programming codes are also transmitted to the microprocessor, the whole access process of accessing these requested programming code can be speeded up accordingly. Applicants believe that the specification has clearly disclosed how the access process becomes faster.

4. Rejections: 35 U.S.C. 112, 2nd PARAGRAPH

Claims 1-38 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a) the claim language does not explain how the operating speed of a microprocessor is

dynamically adjusted;

Response:

In this application, the operating speed is not fixed. Regarding amended claims 1, 8, and 16, the operating speed is reduced when the requested digital data is not stored in the buffering/controlling device, and the operating speed is held when the requested digital data is stored in the buffering/controlling device. The feature of dynamically adjusting the operating speed of the microprocessor has been clearly defined according to the claim language.

b) it is unclear as to what is meant by the data being either 'well prepared' or 'not well prepared';

Response:

Claims 1, 8, and 16 have been amended to remove these unclear definitions.

c) the claims state the executing speed of the microprocessor is either lower than the normal speed or suspended, however, nothing is given in the specification for performing this action;

Response:

As stated in specification paragraph [0027], "The buffering/controlling device 38 outputs an operating clock to the microprocessor 30 so as to slow down/stop microprocessor 30; that is, when the operating clock disappears, the operations of the microprocessor 30 will suspend, when the operating clock slow down, the operations of the microprocessor 30 will also slow down," it is clear that the claimed feature of controlling the executing speed has been fully supported by the specification since controlling the operating clock of the microprocessor is equivalent to controlling the executing speed of the microprocessor.

d) an external circuit or a circuit installed in the microprocessor is never described in such a way that one of ordinary skill would know how to make and use it;

Response:

As disclosed in this application, adjusting an executing speed can be achieved by adjusting an operating clock using an external circuit or a circuit installed in the microprocessor; achieved by inserting an NOP (No Operation) command among commands; or achieved by keeping a program counter unchanged. It should be noted that adjusting an operating clock using an external circuit is equivalent to using the buffering/controlling device to control the operating clock of the microprocessor. Additionally, after reading the specification of this application, a person skilled in this art can readily appreciate that inserting an NOP (No Operation) command among commands or keeping a program counter unchanged can be implemented to adjust the executing speed of the microprocessor.

e) it is unclear as to what is meant by 'access a predetermined number of digital data', is this bits of data, bytes of data, data words or data addresses;

Response:

Referring to specification paragraph [0027], "The buffering/controlling device 38 can consecutively access a predetermined number of programming codes in the serial flash memory 32...If the buffering/controlling device 38 stores the programming codes required by the microprocessor 30, the microprocessor 30 directly receives the desired programming codes from the buffering/controlling device 38", and specification paragraph [0034], "Utilize the buffering/controlling device to access a predetermined number of digital data stored in the serial flash memory or the random access memory . In the embodiment shown in Fig.3, Fig.4, Fig.9 and Fig.10, the buffering/controlling device can consecutively access the predetermined number of

programming codes at a starting address in the serial flash memory or the random access memory," it is clear that accessing a predetermined number of digital data is meant by retrieving data bits, data bytes, or data words of the digital data.

f) it is not clear as to how that data being stored in the buffering/controlling device relates to reducing the operating speed of the microprocessor;

Response:

As clearly stated in claims 1, 8, and 16, the operating speed of the microprocessor is reduced when the desired data requested by the microprocessor is not stored in the buffering/controlling device. Therefore, it is clear that whether the operating speed of the microprocessor is reduced depends upon the existence of the requested data in the buffering/controlling device.

g) what element is used in 'recovering the operating speed' of the microprocessor;

Response:

As disclosed in the specification, the buffering/controlling device is implemented to reduce the operating clock or recover the operating clock. However, according to the claim language, applicants claim the step of recovering the operating clock and this step is fully supported by Fig. 5 and specification paragraph [0030]. Applicants assert that there is no need to further narrow down the claim scope by pointing out what element is used in recovering the operating clock since the claim language is clear.

h) the buffering/controlling device is claimed as being either a FIFO, DRAM, or SRAM, however, these are memory elements and themselves cannot provide control functions.

Response:

Claims 7, 14, 22, and 37 have been amended to claim that the buffering/controlling device comprises a FIFO, DRAM, or SRAM.

Sincerely yours,

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Winston Hsu, Patent Agent No. 41,526
P.O. BOX 506, Merrifield, VA 22116, U.S.A.
Voice Mail: 302-729-1562
Facsimile: 806-498-6673
e-mail : winstonhsu@naipo.com

Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)